ABSTRACT OF THE DISCLOSURE

A static random access memory cell comprising a first invertor including a first p-channel pullup transistor, and a first n-channel pulldown transistor in series with the first p-channel pullup transistor; a second invertor including a second p-channel pullup transistor, and a second n-channel pulldown transistor in series with the second n-channel pullup transistor, the first invertor being cross-coupled with the second invertor, the first and second pullup transistors sharing a common active area; a first access transistor having an active terminal connected to the first invertor; a second access transistor having an active terminal connected to the second invertor; and an isolator isolating the first pullup transistor from the second pullup transistor.